

A VERSATILE HIGH PERFORMANCE
COMPUTER FOR EVERY APPLICATION

ON-BOARD COMPUTER- SYSTEM ARCHITECTURE

Computer systems for space flight applications require ever increasing amounts of computing power to enable (on-the-fly) preprocessing of large data sets from sophisticated experiments and payloads, or even to perform realtime computation of safety-critical control commands. Without this, spacecrafts would be unable to perform complex docking maneuvers or landing approaches autonomously. Besides meeting high performance requirements, the on-board computer systems must also fulfill connectivity criteria. This includes providing interfaces that allow their embedment in a spacecraft's often redundant communications infrastructure or supporting redundant ports for instruments with very high data transfer rates in the gigabit range.

With this in mind, the On-Board Computer-System Architecture (OBC-SA) project developed an architectural framework for future on-board computer systems. It enables the modular integration of systems with different performance and functional characteristics into the IT infrastructure of a spacecraft. To this end, Fraunhofer FOKUS developed a system consisting of two fault-tolerant on-board computers. These computers are based on a DMR system (dual modular redundancy) with the high-end P4080 embedded multicore processor from NXP. They use the PikeOS real-time operating system, which also supports the partitioning of the P4080 processor's resources. Also developed is a Router Board, implementing a redundant interconnect network that enables further computers and subsystems to be hooked up quickly and easily. The Router Board is based on the RTG4 FPGAs (Field Programmable Gate Array) from Microsemi.

COMPACT PCI® SERIAL SPACE

The compact and robust design of the OBC-SA framework is based on the new and open Compact PCI® Serial Space industrial standard (cPCI®). The cPCI® Serial Space backplane provides communication connections for all subsystems. The OBC-SA framework and the modular design of the cPCI® Serial Space standard allow for easy configuration of future on-board computer systems from different computer and I/O components. This means that functionality, computing power, redundancy and I/O interfaces can be flexibly adapted to mission-specific requirements.

P4080 MULTICORE-PROCESSOR

The fault-tolerant on-board computer developed by Fraunhofer FOKUS is based on the P4080, an 8-core CPU of the »QorIQ« PowerPC multicore family from NXP. The processor can be operated at a clock speed of up to 1.5 GHz, thus theoretically reaching a maximum speed of approximately 60 GIPS (giga instructions per second). The P4080 processor benefits from the low-power silicon-on-insulator (SOI) technology, which is also less radiation-sensitive than conventional CMOS technology. The project has validated the system's lower radiation sensitivity to the total ionizing dose (TID) and single event upsets (SEUs) in a number of irradiation tests. The SOI technology is also largely latch-up-free. Furthermore, the P4080 offers the advantages of a highly integrated embedded processor: all important functions are already integrated on-chip, which made it possible to implement an entire compute node on a single 3U cPCI® Serial Space board.

CONTACT

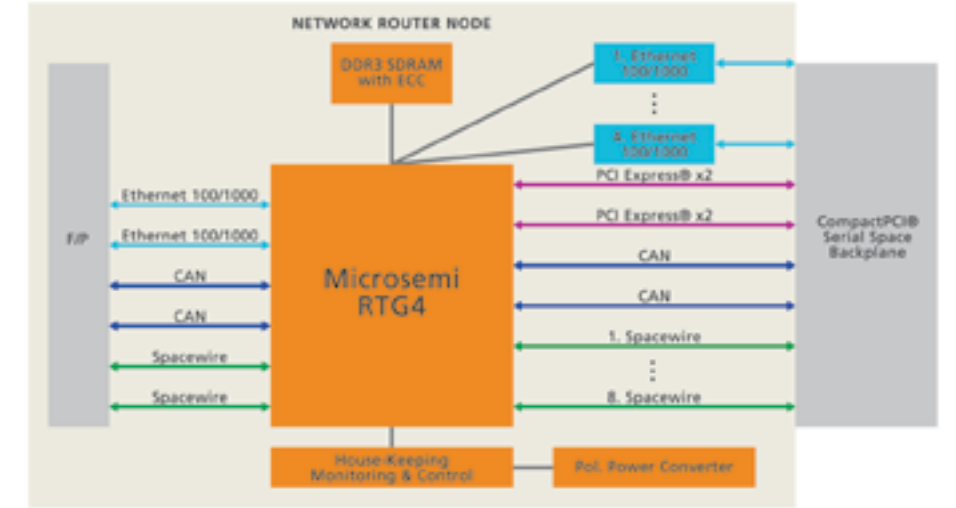
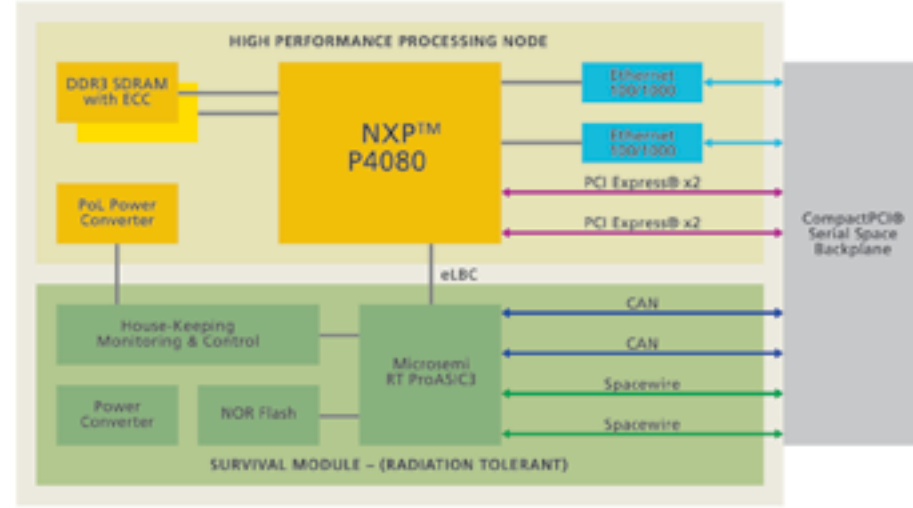
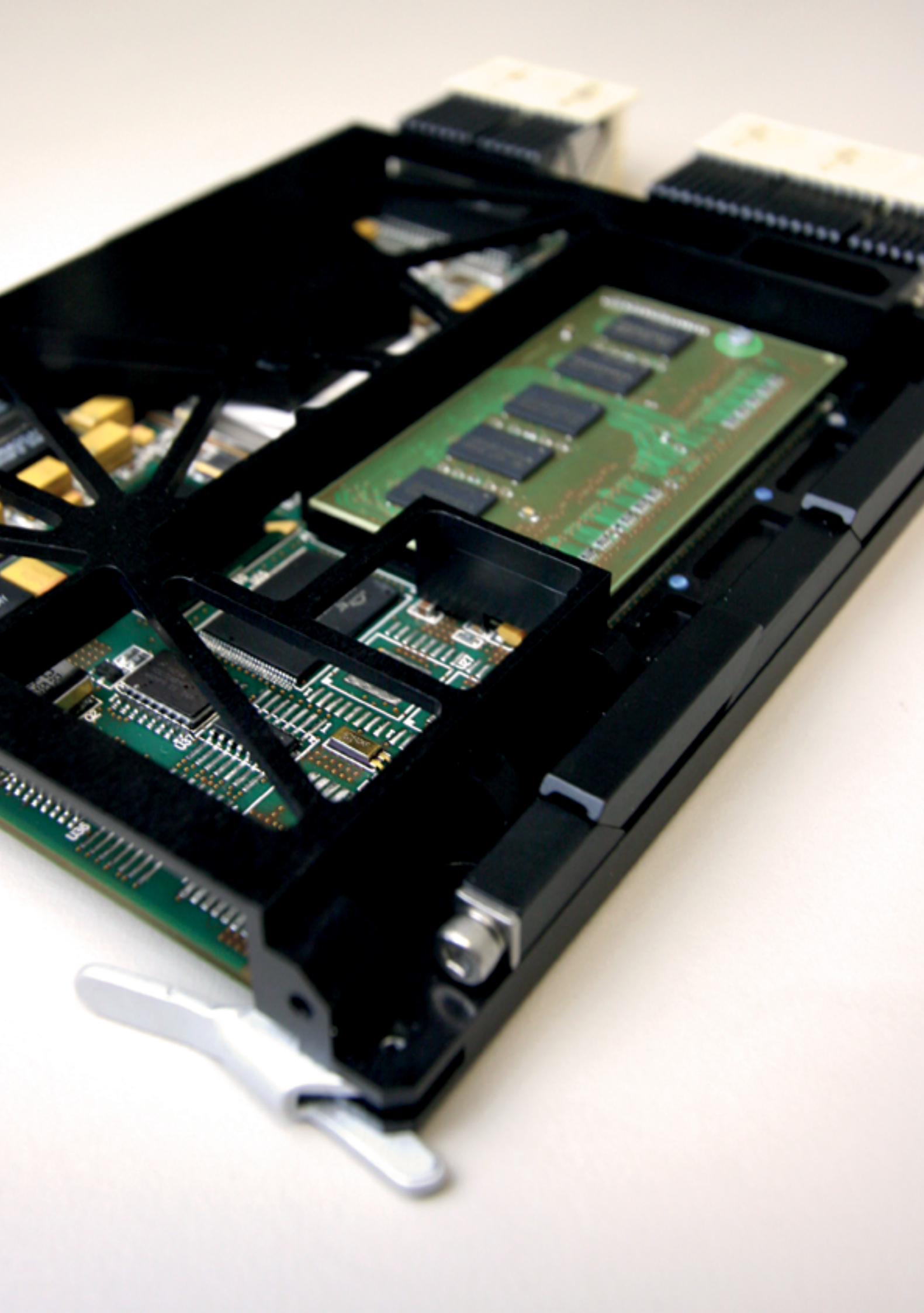
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ON-BOARD COMPUTER- SYSTEM ARCHITECTURE



CPU

Rugged Standard	Open Standard for future Space Computer Systems PICMG® CPCI-S.1 R1.0 CompactPCI® Serial Space, 3U form factor
Fault Tolerance	DMR architecture: Two redundant processing nodes are connected to the redundant communication infrastructure
High Performance	P4080 »QorIQ®« Multi-Core Processor (NXP, E2V) with eight e500mc PowerPC cores @ 1.5 GHz, 60 GIPS, 12 GFLOPS
Memory	Two DDR3 memory banks, 4 GByte each, EDAC protection, soldered
Flash	64 Mbyte NOR flash memory stack (3D Plus), 8 modules, radiation tolerant
Platform FPGA	RT ProASIC®3 (Microsemi) radiation hard by TMR logic
Interfaces	cPCI Serial Space™ compliant rear I/O to redundant network router nodes (Gbit Ethernet, SpaceWire, PCIe x2, CAN)
Debug support	Test and debug interfaces to separate diagnosis board (rear I/O)
Assembly	Standard CompactPCI® Serial Space backplane, robust assembly and effective cooling through CCA clamshell
FDIR	Effective SEU mitigation, Independent hardware watchdog (Platform FPGA), Monitoring of housekeeping data (Platform FPGA), Mutual monitoring of redundant nodes via RMAP protocol
Qualification Status	Qualification status: EQM (TRL 6–7)
Software	U-Boot, board support packages for PikeOS and Linux

ROUTER

Rugged Standard	Open Standard for future Space Computer Systems PICMG® CPCI-S.1 R1.0 CompactPCI® Serial Space, 3U form factor
Fault Tolerance	Two network router nodes provide redundant communication infrastructures
High Connectivity	Gbit Ethernet Router, up to 6 channels, SpaceWire Router, star connection, up to 10 channels, Two PCIe x2 endpoints for specific slots, Four CAN Bus connections, AHB on chip interconnect
Gateway Funktion	Routing among SpaceWire and PCI Express® via AHB
Network Memory	2 GByte DDR3 shared network memory, EDAC protection, soldered
Front Interfaces	2 x GBit Ethernet, 2 x SpaceWire, 2 x CAN Bus
House Keeping Data	Gathering and monitoring of housekeeping data, accessible via SpaceWire RMAP protocol
Debug support	Test and debug interfaces to separate diagnosis board (rear I/O)
Assembly	Standard CompactPCI® Serial Space backplane, robust assembly and effective cooling through CCA clamshell
Radiation Tolerance	TID: tolerance up to 160 krad (RTG4) SEU/SEL immune up to LET 103 MeV*cm²/mg (RTG4)
Router Management	Configuration via SpaceWire RMAP protocol
Qualification Status	Qualification status: EQM (TRL 6–7)